What is claimed is:

1. A memory array comprising:

two or more layers of memory material, each layer of memory material comprising an array of memory cells; and

a first contact penetrating through each layer of memory material in a first plane and electrically connected to each layer of memory material so as to electrically interconnect the layers of memory material in the first plane.

2. The memory array of claim 1, further comprising a dielectric layer disposed between successive layers of memory material.

3. The memory array of claim 1, further comprising:

a select transistor disposed on a substrate of the memory array below the layers of memory material; and

a conductive plug connecting a first source/drain region of the select transistor to a conductive layer located above the layers of memory material, wherein a second source/drain region of the select transistor is connected to the first contact.

4. The memory array of claim 1, further comprising a second contact penetrating through each of the layers of memory material in a second plane substantially perpendicular to the first plane so as to electrically interconnect the layers of memory material in the second plane.

5. The memory array of claim 4, further comprising:

a select transistor disposed on a substrate of the memory array below the layers of memory material; and

a conductive connecting a first source/drain region of the select transistor to a conductive layer located above the layers of memory material, wherein a second source/drain region of the select transistor is connected to the second contact.

6. The memory array of claim 4, further comprising a select transistor disposed on each layer of memory material between the memory cells and the second contact.

7. The memory array of claim 1, further comprising:

a second contact penetrating through one of the layers of memory material in a second plane substantially perpendicular to the first plane and electrically connected thereto; and

a third contact penetrating through another of the layers of memory material in the second plane and electrically connected thereto.

8. The memory array of claim 7, further comprising:

first and second select transistors disposed on a substrate of the memory array below the layers of memory material;

a first conductive plug connecting a first source/drain region of the first select transistor to a conductive layer located above the layers of memory material, wherein a second source/drain region of the first select transistor is connected to the second contact; and

a second conductive plug connecting a first source/drain region of the second select transistor to the conductive layer located above the layers of memory material, wherein a second source/drain region of the second select transistor is connected to the third contact.

9. The memory array of claim 1, wherein each of the memory cells is a floating gate transistor.

10. The memory array of claim 1, wherein each of the memory cells is a silicon-on-sapphire transistor, silicon-on-insulator transistor, thin film transistor, thermoelectric polymer transistor, or silicon-oxide-nitride-oxide-silicon transistor.

11. The memory array of claim 1, wherein each array of memory cells is a NAND flash memory array or a NOR flash memory array.

12. The memory array of claim 1, wherein the memory array is a read only memory array or a static random access memory array.

13. The memory array of claim 1, wherein the layers of memory material comprise polysilicon.

14. A memory array comprising:

a plurality of layers of memory material, each layer of memory material containing an array of memory cells arranged in rows and columns and each of the plurality of layers of memory material separated from each other by a dielectric material;

a plurality of first contacts passing through each of the plurality of layers of memory material, each first contact in electrical communication with at least one memory cell of a column of memory cells in each of the plurality of layers of memory material;

a plurality of second contacts passing through each of the plurality of layers of memory material, each second contact in selective electrical communication with a row of memory cells in each of the plurality of layers of memory material; and

a plurality of first select transistors, each first select transistor connected between a second contact and its respective row of memory cells for providing selective electrical communication, the plurality of first select transistors adapted to provide electrical communication with only one row of memory cells for each second contact.

15. The memory array of claim 14, further comprising for each first contact:

one second select transistor disposed on a substrate of the memory array below the layers of memory material; and

one first conductive plug passing through the memory array and connecting a first source/drain region of the second select transistor to a global bit line located above the layers of memory material, wherein a second source/drain region of the second select transistor is connected to the first contact.

16. The memory array of claim 15, further comprising for each second contact:

one third select transistor disposed on the substrate below the layers of memory material; and

one second conductive plug connecting a first source/drain region of the third select transistor to a global row line located above the layers of memory material, wherein a second source/drain region of the third select transistor is connected to the second contact.

17. The memory array of claim 14, wherein each of the memory cells is a flash memory cell.

18. The memory array of claim 14, wherein each of the memory cells is a silicon-on-sapphire transistor, silicon-on-insulator transistor, thin film transistor, thermoelectric polymer transistor, or silicon-oxide-nitride-oxide-silicon transistor.

19. The memory array of claim 14, wherein the array of memory cells of each layer of memory material is a NAND flash memory array or a NOR flash memory array.

20. The memory array of claim 14, wherein the memory array is a read only memory array or a static random access memory array.

21. The memory array of claim 14, further comprising a plurality of second select transistors, each second select transistor connected between a first contact and its respective column of memory cells for providing selective electrical communication, wherein each first contact is connected directly to a global bit line located above the layers of memory material.

22. The memory array of claim 14, wherein each second contact is connected directly to a global row line located above the layers of memory material.

23. The memory array of claim 14, wherein each first contact electrically connects NAND strings of the respective layers of memory material.

24. The memory array of claim 14, wherein each first contact electrically connects drain regions of memory cells of the respective layers of memory material.

25. A memory array comprising:

a plurality of layers of memory material, each layer of memory material containing an array of memory cells arranged in rows and columns and each of the plurality of layers of memory material separated from each other by a dielectric material;

a plurality of first contacts passing through each of the plurality of layers of memory material, each first contact in electrical communication with at least one memory cell of a row of memory cells in each of the plurality of layers of memory material;

a plurality of second contacts passing through each of the plurality of layers of memory material, each second contact in selective electrical communication with a column of memory cells in each of the plurality of layers of memory material; and

a plurality of first select transistors, each first select transistor connected between a second contact and its respective column of memory cells for providing selective electrical communication, the plurality of first select transistors adapted to provide electrical communication with only one column of memory cells for each second contact.

26. The memory array of claim 25, further comprising for each first contact:

one second select transistor disposed on a substrate of the memory array below the layers of memory material; and

one first conductive plug connecting a first source/drain region of the second select transistor to a global row line located above the layers of memory material, wherein a second source/drain region of the second select transistor is connected to the first contact.

27. The memory array of claim 26, further comprising for each second contact:

one third select transistor disposed on the substrate below the layers of memory material; and

one second conductive plug connecting a first source/drain region of the third select transistor to a global bit line located above the layers of memory material, wherein a second source/drain region of the third select transistor is connected to the second contact.

28. The memory array of claim 25, further comprising a plurality of second select transistors, each second select transistor connected between a first contact and its respective row of memory cells for providing selective electrical communication, wherein each first contact is connected directly to a global row line located above the layers of memory material.

29. The memory array of claim 25, wherein each second contact is connected directly to a global bit line located above the layers of memory material.

30. The memory array of claim 25, wherein each of the memory cells is a flash memory cell.

31. The memory array of claim 25, wherein each of the memory cells is a silicon-on-sapphire transistor, silicon-on-insulator transistor, thin film transistor, thermoelectric polymer transistor, or silicon-oxide-nitride-oxide-silicon transistor.

32. The memory array of claim 25, wherein the array of memory cells of each layer of memory material is a NAND flash memory array or a NOR flash memory array.

33. The memory array of claim 25, wherein the memory array is a read only memory array or a static random access memory array.

34. The memory array of claim 25, wherein the second contact electrically connects NAND strings of the respective layers of memory material.

35. The memory array of claim 25, wherein the second contact electrically connects drain regions of memory cells of the respective layers of memory material.

36. A memory array comprising:

first and second layers of memory material, each of the first and second layers of memory material containing an array of memory cells arranged in rows and columns and the first and second layers of memory material separated from each other by a dielectric material;

a plurality of first contacts passing through the first and second layers of memory material, each first contact in electrical communication with at least one memory cell of a column of memory cells in each of the first and second layers of memory material;

a plurality of second contacts passing through the first layer of memory material, each second contact in selective electrical communication with a row of memory cells of the first layer of memory material; and

a plurality of third contacts passing through the second layer of memory material, each third contact in selective electrical communication with a row of memory cells of the second layer of memory material.

37. The memory array of claim 36, further comprising for each first contact:

one first select transistor disposed on a substrate of the memory array below the layers of memory material; and

one first conductive plug connecting a first source/drain region of the first select transistor to a global bit line located above the layers of memory material, wherein a second source/drain region of the first select transistor is connected to the first contact.

38. The memory array of claim 37, further comprising for each second contact:

one second select transistor disposed on the substrate below the layers of memory material; and

one second conductive plug connecting a first source/drain region of the second select transistor to a global row line located above the layers of memory material, wherein a second source/drain region of the second select transistor is connected to the second contact.

39. The memory array of claim 38, further comprising for each third contact:

one third select transistor disposed on the substrate below the layers of memory material; and

one third conductive plug connecting a first source/drain region of the third select transistor to the global row line, wherein a second source/drain region of the third select transistor is connected to the third contact.

40. The memory array of claim 36, further comprising a plurality of select transistors, each select transistor connected between a first contact and its respective column of memory cells for providing selective electrical communication, wherein each first contact is connected directly to a global bit line located above the layers of memory material.

41. The memory array of claim 36, further comprising:

a plurality of first select transistors, each first select transistor connected between a second contact and its respective row of memory cells for providing selective electrical communication, wherein each second contact is connected directly to a global row line located above the layers of memory material; and

a plurality of second select transistors, each second select transistor connected between a third contact and its respective row of memory cells for providing selective electrical communication, wherein each third contact is connected directly to a global row line located above the layers of memory material.

42. The memory array of claim 36, wherein each of the memory cells is a silicon-on-sapphire transistor, silicon-on-insulator transistor, thin film transistor, thermoelectric polymer transistor, or silicon-oxide-nitride-oxide-silicon transistor.

43. The memory array of claim 36, wherein the array of memory cells of each layer of memory material is a NAND flash memory array or a NOR flash memory array.

44. The memory array of claim 36, wherein the memory array is a read only memory array or a static random access memory array.

45. The memory array of claim 36, wherein the first contact electrically connects NAND strings of the respective layers of memory material.

46. The memory array of claim 36, wherein the first contact electrically connects drain regions of memory cells of the respective layers of memory material.

47. A memory array comprising:

first and second layers of memory material, each of the first and second layers of memory material containing an array of memory cells arranged in rows and columns and the first and second layers of memory material separated from each other by a dielectric material;

a plurality of first contacts passing through the first and second layers of memory material, each first contact in electrical communication with at least one memory cell of a row of memory cells in each of the first and second layers of memory material;

a plurality of second contacts passing through the first layer of memory material, each second contact in selective electrical communication with a column of memory cells of the first layer of memory material; and

a plurality of third contacts passing through the second layer of memory material, each third contact in selective electrical communication with a column of memory cells of the second layer of memory material.

48. The memory array of claim 47, further comprising for each first contact:

one first select transistor disposed on a substrate of the memory array below the layers of memory material; and

one first conductive plug connecting a first source/drain region of the first select transistor to a global row line located above the layers of memory material, wherein a second source/drain region of the first select transistor is connected to the first contact.

49. The memory array of claim 48, further comprising for each second contact:

one second select transistor disposed on the substrate below the layers of memory material; and

one second conductive plug connecting a first source/drain region of the second select transistor to a global bit line located above the layers of memory material, wherein a second source/drain region of the second select transistor is connected to the second contact.

50. The memory array of claim 49, further comprising for each third contact:

one third select transistor disposed on the substrate below the layers of memory material; and

one third conductive plug connecting a first source/drain region of the third select transistor to the global bit line, wherein a second source/drain region of the third select transistor is connected to the third contact.

51. The memory array of claim 47, further comprising a plurality of select transistors, each select transistor connected between a first contact and its respective row of memory cells for providing selective electrical communication, wherein each first

contact is connected directly to a global row line located above the layers of memory material.

52. The memory array of claim 47, further comprising:

a plurality of first select transistors, each first select transistor connected between a second contact and its respective column of memory cells for providing selective electrical communication, wherein each second contact is connected directly to a global bit line located above the layers of memory material; and

a plurality of second select transistors, each second select transistor connected between a third contact and its respective column of memory cells for providing selective electrical communication, wherein each third contact is connected directly to a bit row line located above the layers of memory material.

53. The memory array of claim 47, wherein each of the memory cells is a silicon-on-sapphire transistor, silicon-on-insulator transistor, thin film transistor, thermoelectric polymer transistor, or silicon-oxide-nitride-oxide-silicon transistor.

54. The memory array of claim 47, wherein the array of memory cells of each layer of memory material is a NAND flash memory array or a NOR flash memory array.

55. The memory array of claim 47, wherein the memory array is a read only memory array or a static random access memory array.

56. A method of forming a memory array, comprising:

forming a stack of two or more layers of memory material on a substrate, each layer of memory material having an array of memory cells; and

forming one or more contacts that pass through each of the layers of memory material.

57. The method of claim 56, further comprising connecting a first contact of the one or more contacts to a first conductive line located above the layers of memory material.

58. The method of claim 57, further comprising connecting a second contact of the one or more contacts to a second conductive line located above the layers of memory material.

59. A method of forming a memory array, comprising:

forming a stack of two or more layers of memory material on a substrate, each layer of memory material having an array of memory cells and separated from another layer of memory material by a dielectric layer;

forming a first contact that passes through each layer of memory material in a first plane to electrically interconnect the layers of memory material in the first plane; and

forming a second contact that passes through at least one of the layers of memory material in a second plane that is substantially perpendicular to the first plane.

60. The method of claim 59, further comprising connecting the first contact to a first conductive line located above the layers of memory material, wherein connecting the first contact to the first conductive line comprises:

forming a first select transistor on the substrate;

connecting a first source/drain region of the first select transistor to the first contact; and

forming a first conductive plug to interconnect a second source/drain region of the first select transistor to the first conductive line.

61. The method of claim 60, further comprising connecting the second contact to a second conductive line located above the layers of memory material, wherein connecting the second contact to the second conductive line comprises:

forming a second select transistor on the substrate;

connecting a first source/drain region of the second select transistor to the second contact; and

forming a second conductive plug to interconnect a second source/drain region of the second select transistor to the second conductive line.

62. The method of claim 59, wherein forming a second contact that passes through at least one of the layers of memory material in a second plane comprises forming a second contact that passes through each layer of memory material to electrically interconnect the layers of memory material in the second plane and further comprising forming a select transistor on each layer of memory material between the memory cells of the respective layers of memory material and the second contact.

63. The method of claim 59, wherein forming a stack of two or more layers of memory material on a substrate comprises forming two layers of memory material, wherein forming a second contact that passes through at least one of the layers of memory material in a second plane comprises forming a second contact that passes through only a first of the two layers of memory material, and further comprising forming a third contact that passes through only a second of the two layers of memory material.

64. A method of forming a memory array, comprising:

forming a stack of a plurality of alternating layers of memory material and dielectric layers on a substrate;

forming an array of memory cells arranged in rows and columns on each layer of memory material; forming a plurality of first contacts passing through each of the plurality of layers of memory material so that each first contact is in electrical communication with at least one memory cell of a column of memory cells in each of the plurality of layers of memory material;

forming a plurality of second contacts passing through each of the plurality of layers of memory material so that each second contact is in selective electrical communication with a row of memory cells in each of the plurality of layers of memory material; and

forming a plurality of first select transistors such that each first select transistor is connected between a second contact and its respective row of memory cells for providing selective electrical communication, the plurality of first select transistors adapted to provide electrical communication with only one row of memory cells for each second contact.

65. The method of claim 64, further comprising forming a plurality of global bit lines and global row lines above the layers of memory material, each global bit line in electrical communication with at least one of the first contacts and each global row line in electrical communication with at least one of the second contacts.

66. The method of claim 65, further comprising connecting each global bit line to its respective first contact, wherein connecting a global bit line to a first contact comprises:

forming a second select transistor on the substrate;

connecting a first source/drain region of the second select transistor to the first contact; and

forming a first conductive plug to interconnect a second source/drain region of the second select transistor to the global bit line.

67. The method of claim 66, further comprising connecting each global row line to its respective second contact, wherein connecting a global row line to a second contact comprises:

forming a third select transistor on the substrate;

connecting a first source/drain region of the third select transistor to the second contact; and

forming a second conductive plug to interconnect a second source/drain region of the third select transistor to the global row line.

68. The method of claim 64, further comprising:

forming a plurality of second select transistors such that each second select transistor is connected between a first contact and its respective column of memory cells for providing selective electrical communication; and

connecting each first contact directly to a respective one of a plurality of global bit lines formed above the layers of memory material.

69. The method of claim 64, further comprising connecting each second contact connected directly to a respective one of a plurality of global row lines formed on a dielectric layer above the layers of memory material.

70. The method of claim 64, wherein forming an array of memory cells comprises forming a floating gate transistor for each memory cell.

71. The method of claim 70, wherein forming a floating gate transistor for each memory cell comprises forming each floating gate transistor using silicon-on-sapphire, silicon-on-insulator, thin film transistor, thermoelectric polymer, or silicon-oxide-nitride-oxide-silicon technology.

72. A method of forming a memory array, comprising:

forming a stack of a plurality of alternating layers of memory material and dielectric layers on a substrate;

forming an array of memory cells arranged in rows and columns on each layer of memory material;

forming a plurality of first contacts passing through each of the plurality of layers of memory material so that each first contact is in electrical communication

with at least one memory cell of a row of memory cells in each of the plurality of layers of memory material;

forming a plurality of second contacts passing through each of the plurality of layers of memory material so that each second contact is in selective electrical communication with a column of memory cells in each of the plurality of layers of memory material; and

forming a plurality of first select transistors such that each first select transistor is connected between a second contact and its respective column of memory cells for providing selective electrical communication, the plurality of first select transistors adapted to provide electrical communication with only one column of memory cells for each second contact.

73. The method of claim 72, further comprising forming a plurality of global bit lines and global row lines above the layers of memory material, each global bit line in electrical communication with at least one of the second contacts and each global row line in electrical communication with at least one of the first contacts.

74. The method of claim 73, further comprising connecting each global row line to its respective first contact, wherein connecting a global row line to a first contact comprises:

forming a second select transistor on the substrate;

connecting a first source/drain region of the second select transistor to the first contact; and

forming a first conductive plug to interconnect a second source/drain region of the second select transistor to the global row line.

75. The method of claim 74, further comprising connecting each global bit line to its respective second contact, wherein connecting a global bit line to a second contact comprises:

forming a third select transistor on the substrate;

connecting a first source/drain region of the third select transistor to the second contact; and

forming a second conductive plug to interconnect a second source/drain region of the third select transistor to the global bit line.

76. The method of claim 72, further comprising:

forming a plurality of second select transistors such that each second select transistor is connected between a first contact and its respective row of memory cells for providing selective electrical communication; and

connecting each first contact directly to a respective one of a plurality of global row lines formed on a dielectric layer above the layers of memory material.

77. The method of claim 72, further comprising connecting each second contact connected directly to a respective one of a plurality of global bit lines formed on a dielectric layer above the layers of memory material.

78. The method of claim 72, wherein forming an array of memory cells comprises forming a floating gate transistor for each memory cell.

79. The method of claim 78, wherein forming a floating gate transistor for each memory cell comprises forming each floating gate transistor using silicon-on-sapphire, silicon-on-insulator, thin film transistor, thermoelectric polymer, or silicon-oxide-nitride-oxide-silicon technology.

80. A method of forming a memory array, comprising:

forming a stack of alternating layers of memory material and dielectric layers on a substrate, wherein the stack comprises two layers of memory material;

forming an array of memory cells arranged in rows and columns on each of the two layers of memory material;

forming a plurality of first contacts passing through each of the two layers of memory material so that each first contact is in electrical communication with at least one memory cell of a column of memory cells in each of the two layers of memory material;

forming a plurality of second contacts passing through a first layer of the two layers of memory material, each second contact in selective electrical communication with a row of memory cells of the first layer; and

forming a plurality of third contacts passing through a second layer of the two layers of memory material, each third contact in selective electrical communication with a row of memory cells of the second layer.

81. The method of claim 80, further comprising forming a plurality of global bit lines and global row lines above the layers of memory material, each global bit line in electrical communication with at least one of the first contacts and each global row line in electrical communication with at least one of the second contacts and at least one of the third contacts.

82. The method of claim 81, further comprising connecting each global bit line to its respective first contact, wherein connecting a global bit line to a first contact comprises:

forming a first select transistor on the substrate;

connecting a first source/drain region of the first select transistor to the first contact; and

forming a first conductive plug to interconnect a second source/drain region of the first select transistor to the global bit line.

83. The method of claim 82, further comprising connecting each global row line to its respective second contact, wherein connecting a global row line to a second contact comprises:

forming a second select transistor on the substrate;

connecting a first source/drain region of the second select transistor to the second contact; and

forming a second conductive plug to interconnect a second source/drain region of the second select transistor to the global row line.

84. The method of claim 83, further comprising connecting each global row line to its respective third contact, wherein connecting a global row line to a third contact comprises:

forming a third select transistor on the substrate;

connecting a first source/drain region of the third select transistor to the third contact; and

forming a third conductive plug to interconnect a second source/drain region of the third select transistor to the global row line.

85. The method of claim 80, further comprising:

forming a plurality of select transistors such that each select transistor is connected between a first contact and its respective column of memory cells for providing selective electrical communication; and

connecting each first contact directly to a respective one of a plurality of global bit lines formed on a dielectric layer above the layers of memory material.

86. The method of claim 80, further comprising:

forming a plurality of first select transistors such that each first select transistor is connected between a second contact and its respective row of memory cells for providing selective electrical communication;

connecting each second contact directly to a respective one of a plurality of global row lines formed on a dielectric layer above the layers of memory material;

forming a plurality of second select transistors such that each second select transistor is connected between a third contact and its respective row of memory cells for providing selective electrical communication; and

connecting each third contact directly to a respective one of the plurality of global row lines.

87. The method of claim 80, wherein forming an array of memory cells comprises forming a floating gate transistor for each memory cell.

88. The method of claim 87, wherein forming a floating gate transistor for each memory cell comprises forming each floating gate transistor using silicon-on-sapphire, silicon-on-insulator, thin film transistor, thermoelectric polymer, or silicon-oxide-nitride-oxide-silicon technology.

89. A method of forming a memory array, comprising:

forming a stack of alternating layers of memory material and dielectric layers on a substrate, wherein the stack comprises two layers of memory material;

forming an array of memory cells arranged in rows and columns on each of the two layers of memory material;

forming a plurality of first contacts passing through each of the two layers of memory material so that each first contact is in electrical communication with at least one memory cell of a row of memory cells in each of the two layers of memory material;

forming a plurality of second contacts passing through a first layer of the two layers of memory material, each second contact in selective electrical communication with a column of memory cells of the first layer; and

forming a plurality of third contacts passing through a second layer of the two layers of memory material, each third contact in selective electrical communication with a column of memory cells of the second layer.

90. The method of claim 89, further comprising forming a plurality of global bit lines and global row lines above the layers of memory material, each global row line in electrical communication with at least one of the first contacts and each global bit line in electrical communication with at least one of the second contacts and at least one of the third contacts.

91. The method of claim 90, further comprising connecting each global row line to its respective first contact, wherein connecting a global row line to a first contact comprises:

forming a first select transistor on the substrate;

connecting a first source/drain region of the first select transistor to the first contact; and

forming a first conductive plug to interconnect a second source/drain region of the first select transistor to the global row line.

92. The method of claim 91, further comprising connecting each global bit line to its respective second contact, wherein connecting a global bit line to a second contact comprises:

forming a second select transistor on the substrate;

connecting a first source/drain region of the second select transistor to the second contact; and

forming a second conductive plug to interconnect a second source/drain region of the second select transistor to the global bit line.

93. The method of claim 92, further comprising connecting each global bit line to its respective third contact, wherein connecting a global bit line to a third contact comprises:

forming a third select transistor on the substrate;

connecting a first source/drain region of the third select transistor to the third contact; and

forming a third conductive plug to interconnect a second source/drain region of the third select transistor to the global bit line.

94. The method of claim 89, further comprising:

forming a plurality of select transistors such that each select transistor is connected between a first contact and its respective row of memory cells for providing selective electrical communication; and

connecting each first contact directly to a respective one of a plurality of global row lines formed on a dielectric layer above the layers of memory material.

95. The method of claim 89, further comprising:

forming a plurality of first select transistors such that each first select transistor is connected between a second contact and its respective column of memory cells for providing selective electrical communication;

connecting each second contact directly to a respective one of a plurality of global bit lines formed on a dielectric layer above the layers of memory material;

forming a plurality of second select transistors such that each second select transistor is connected between a third contact and its respective column of memory cells for providing selective electrical communication; and

connecting each third contact directly to a respective one of the plurality of global bit lines.

96. A memory device comprising:

a multi-layer memory array, wherein the array comprises:

a plurality of layers of memory material, each layer of memory material containing an array of memory cells arranged in rows and columns and each of the plurality of layers of memory material separated from each other by a dielectric material;

a plurality of first contacts passing through each of the plurality of layers of memory material, each first contact in electrical communication with at least one memory cell of a column of memory cells in each of the plurality of layers of memory material;

a plurality of second contacts passing through each of the plurality of layers of memory material, each second contact in selective electrical communication with a row of memory cells in each of the plurality of layers of memory material;

a plurality of first select transistors, each first select transistor connected between a second contact and its respective row of memory cells for providing selective electrical communication, the plurality of first select transistors adapted to provide electrical communication with only one row of memory cells for each second contact; and

a plurality of global bit lines and global row lines above the layers of memory material, each global bit line in electrical communication with at least one of the first contacts and each global row line in electrical communication with at least one of the second contacts;

column access circuitry connected to the plurality of global bit lines; and

row access circuitry connected to the plurality of global row lines.

97. A memory device comprising:

a multi-layer memory array, wherein the array comprises:

a plurality of layers of memory material, each layer of memory material containing an array of memory cells arranged in rows and columns and each of the plurality of layers of memory material separated from each other by a dielectric material;

a plurality of first contacts passing through each of the plurality of layers of memory material, each first contact in electrical communication with at least one memory cell of a row of memory cells in each of the plurality of layers of memory material;

a plurality of second contacts passing through each of the plurality of layers of memory material, each second contact in selective electrical communication with a column of memory cells in each of the plurality of layers of memory material;

a plurality of first select transistors, each first select transistor connected between a second contact and its respective column of memory cells for providing selective electrical communication, the plurality of first select transistors adapted to provide electrical communication with only one column of memory cells for each second contact; and

a plurality of global bit lines and global row lines above the layers of memory material, each global bit line in electrical communication with at least one of the second contacts and each global row line in electrical communication with at least one of the first contacts;

column access circuitry connected to the plurality of global bit lines; and

row access circuitry connected to the plurality of global row lines.

98. A memory device comprising:

a multi-layer memory array, wherein the array comprises:

first and second layers of memory material, each of the first and second layers of memory material containing an array of memory cells arranged in rows and columns and the first and second layers of memory material separated from each other by a dielectric material;

a plurality of first contacts passing through the first and second layers of memory material, each first contact in electrical communication with at least one memory cell of a column of memory cells in each of the first and second layers of memory material;

a plurality of second contacts passing through the first layer of memory material, each second contact in selective electrical communication with a row of memory cells of the first layer of memory material;

a plurality of third contacts passing through the second layer of memory material, each third contact in selective electrical communication with a row of memory cells of the second layer of memory material; and

a plurality of global bit lines and global row lines above the layers of memory material, each global bit line in electrical communication with at least one of the first contacts and each global row line in electrical communication with at least one of the second contacts and at least one of the third contacts;

column access circuitry connected to the plurality of global bit lines; and

row access circuitry connected to the plurality of global row lines.

99. A memory device comprising:

a multi-layer memory array, wherein the array comprises:

first and second layers of memory material, each of the first and second layers of memory material containing an array of memory cells arranged in rows and columns and the first and second layers of memory material separated from each other by a dielectric material;

a plurality of first contacts passing through the first and second layers of memory material, each first contact in electrical communication

with at least one memory cell of a row of memory cells in each of the first and second layers of memory material;

a plurality of second contacts passing through the first layer of memory material, each second contact in selective electrical communication with a column of memory cells of the first layer of memory material;

a plurality of third contacts passing through the second layer of memory material, each third contact in selective electrical communication with a column of memory cells of the second layer of memory material; and

a plurality of global bit lines and global row lines above the layers of memory material, each global row line in electrical communication with at least one of the first contacts and each global bit line in electrical communication with at least one of the second contacts and at least one of the third contacts;

column access circuitry connected to the plurality of global bit lines; and

row access circuitry connected to the plurality of global row lines.

100. An electronic system comprising:

a processor;

a memory device connected to the processor, the memory device comprising:

a multi-layer memory array, wherein the memory array comprises:

a plurality of layers of memory material, each layer of memory material containing an array of memory cells arranged in rows and columns and each of the plurality of layers of memory material separated from each other by a dielectric material;

a plurality of first contacts passing through each of the plurality of layers of memory material, each first contact in electrical communication with at least one memory cell of a column of memory cells in each of the plurality of layers of memory material;

a plurality of second contacts passing through each of the plurality of layers of memory material, each second contact in selective electrical communication with a row of memory cells in each of the plurality of layers of memory material;

a plurality of first select transistors, each first select transistor connected between a second contact and its respective row of memory cells for providing selective electrical communication, the plurality of first select transistors adapted to provide electrical communication with only one row of memory cells for each second contact; and

a plurality of global bit lines and global row lines above the layers of memory material, each global bit line in electrical communication with at least one of the first contacts and each global row line in electrical communication with at least one of the second contacts;

column access circuitry connected to the plurality of global bit lines; and

row access circuitry connected to the plurality of global row lines.

101. An electronic system comprising:

a processor;

a memory device connected to the processor, the memory device comprising:

a multi-layer memory array, wherein the memory array comprises:

a plurality of layers of memory material, each layer of memory material containing an array of memory cells arranged in rows and columns and each of the plurality of layers of memory material separated from each other by a dielectric material;

a plurality of first contacts passing through each of the plurality of layers of memory material, each first contact in electrical communication with at least one memory cell of a row of memory cells in each of the plurality of layers of memory material;

a plurality of second contacts passing through each of the plurality of layers of memory material, each second contact in selective electrical communication with a column of memory cells in each of the plurality of layers of memory material;

a plurality of first select transistors, each first select transistor connected between a second contact and its respective column of memory cells for providing selective electrical communication, the plurality of first select transistors adapted to provide electrical communication with only one column of memory cells for each second contact; and

a plurality of global bit lines and global row lines above the layers of memory material, each global bit line in electrical communication with at least one of the second contacts and each global row line in electrical communication with at least one of the first contacts;

column access circuitry connected to the plurality of global bit lines; and

row access circuitry connected to the plurality of global row lines.

102. An electronic system comprising:

a processor;

a memory device connected to the processor, the memory device comprising:

a multi-layer memory array, wherein the memory array comprises:

first and second layers of memory material, each of the first and second layers of memory material containing an array of memory cells arranged in rows and columns and the first and second layers of memory material separated from each other by a dielectric material;

a plurality of first contacts passing through the first and second layers of memory material, each first contact in electrical communication with at least one memory cell of a column of memory cells in each of the first and second layers of memory material;

a plurality of second contacts passing through the first layer of memory material, each second contact in selective electrical communication with a row of memory cells of the first layer of memory material;

a plurality of third contacts passing through the second layer of memory material, each third contact in selective electrical communication with a row of memory cells of the second layer of memory material; and

a plurality of global bit lines and global row lines above the layers of memory material, each global bit line in electrical communication with at least one of the first contacts and each global row line in electrical communication with at least one of the second contacts and at least one of the third contacts;

column access circuitry connected to the plurality of global bit lines; and

row access circuitry connected to the plurality of global row lines.

103. An electronic system comprising:

a processor;

a memory device connected to the processor, the memory device comprising:

a multi-layer memory array, wherein the memory array comprises:

first and second layers of memory material, each of the first and second layers of memory material containing an array of memory cells arranged in rows and columns and the first and second layers of memory material separated from each other by a dielectric material;

a plurality of first contacts passing through the first and second layers of memory material, each first contact in electrical communication with at least one memory cell of a row of memory cells in each of the first and second layers of memory material;

a plurality of second contacts passing through the first layer of memory material, each second contact in selective electrical communication with a column of memory cells of the first layer of memory material;

a plurality of third contacts passing through the second layer of memory material, each third contact in selective electrical communication with a column of memory cells of the second layer of memory material; and

a plurality of global bit lines and global row lines above the layers of memory material, each global bit line in electrical communication with at least one of the first contacts and each global row line in electrical communication with at least one of the second contacts and at least one of the third contacts;

column access circuitry connected to the plurality of global bit lines; and

row access circuitry connected to the plurality of global row lines.